Remarks

Applicant respectfully requests reconsideration of this application. Claims 50-57 have been canceled. Claims 93-111 are unchanged. No claims have been allowed.

Information Disclosure Statement

Applicant wishes to bring to the attention of the Examiner the existence of the following related applications: Serial No. 10/163,536 filed 6/06/02; Serial No. 10/277,849 filed 10/21/02; Serial No. 10/368,065 filed 02/18/03; and Serial No. 10/368,146 filed 02/18/03.

Double Patenting Rejection

Claims 50-57 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 6,207,994. In view of the cancellation of the subject claims, Applicant submits that this rejection is rendered moot.

Claim Rejections - 35 U.S.C. § 103

Claims 50-53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rumennik et al. (US 5,258,636; "Rumennik") in view of Eklund (US 5,313,082; "Eklund"). Additionally, claims 54 and 57 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rumennik in view of Eklund, and further in view of Yamanishi, et al. (JP404107877A; "Yamanishi"). Claims 55 and 56 were also rejected 35 U.S.C. § 103(a) as being unpatentable over Rumennik in view of Eklund, and further in view of Williams et al. (US 5,386,136; "Williams"). The cancellation of claims 50-57 renders each of these rejections moot.

Claims 93-95 and 99-111 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of Yamanishi and/or Eklund. Additionally, claims 96-98 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams

in view of Yamanishi and/or Eklund, and further in view of Colak (US 4,626,879; "Colak").

Applicant respectfully submits that *prima facie* obviousness is absent because (1) there is no suggestion, teaching, or motivation to modify or combine the cited references so as to arrive at the claimed invention; (2) there is no reasonable expectation of success by the hypothetical person of ordinary skill in the art at the time the invention was made that the proposed combination or modification would work to produce beneficial results; and (3) the prior art fails to teach or suggest all of the elements and limitations recited in the claims.

Williams discloses a lightly doped drain (LDD) lateral MOSFET transistor having reduced peak electric fields at the gate edge due to the presence of a P+ buried layer 501. Buried layer 501 pushes the electrical equipotential lines beneath the silicon surface laterally further and more evenly in the direction of the drain contact region 507. (Col. 6, lines 58-65) Williams does not teach or suggest a HVFET that includes a buried region disposed in an epitaxial layer of opposite conductivity type, which forms conduction channels above and below the buried region, as recited, for example, in claim 93.

Indeed, Williams fails to teach, disclose, or suggest any type of buried layer regions in his drift region 522. Instead, Williams merely teaches a shallow N-drift region 522 formed at the surface of P- epitaxial layer 512. In Figures 5-12 Williams teaches that the depth of N-drift region 522 is the same as that of N+ drain diffusion region 507, which is conventionally about one micron deep. (See attached Rule 1.132 declaration.) By way of dimensional comparison, Williams discloses an optional N-well 506 that surrounds N+ drain diffusion region 507, but not shallow drift region 522, as being 3-12 microns deep. (Col. 6, lines 20-23) On the source side of the transistor Williams teaches a P-body region 503 that is diffused as deep as 4 microns into the substrate. (Col. 5, lines 65-67).

With respect to amended claims 93 and 103, a person of ordinary skill would have lacked any expectation of success in attaining an HVFET with a "conduction channel being formed above the buried region with an impurity concentration of approximately 1 X $10^{12}/cm^{2}$". Neither Yamanishi nor Williams teach, disclose or suggest a HVFET with an upper conduction channel having "an impurity concentration of approximately 1 X $10^{12}/cm^{2}$" as recited, in amended claims 93 and 103. Indeed, Yamanishi is completely silent as to the impurity concentration in his N-type construction at the surface of the substrate.

The existence of first and second conduction channels is certainly not inherent in Yamanishi's device structure. A retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination. An allegedly inherent characteristic must *necessarily* flow from the teachings of the applied prior art. In this case, there is no teaching in Yamanishi (or the other cited prior art) that reasonably supports the conclusion that his device structure necessarily includes first and second conduction channels – much less with the first conduction channel having an impurity concentration of approximately 1 X $10^{12}/cm^{2}$.

Moreover, as the attached Rule 1.132 declaration attests, a person of ordinary skill following the teachings would have lacked any reasonable expectation of success of attaining Applicant's invention since Yamanishi's dopant desegregation processing technique was known to be highly unpredictable and very difficult to control. The declaration further attests to the fact that Yamanishi's device is inoperative to provide a HVFET device with first and second extended drain conduction channels.

Eklund teaches a three-sided, junction-gate, field-effect transistor in series with an insulated-gate, field-effect transistor on the same chip. Eklund, however, does not teach or suggest a high-voltage transistor that includes a buried region

forming conduction channels within an epitaxial layer, one conduction channel being formed above the buried region with an impurity concentration of approximately 1 X $10^{12}/cm^2$ and another conduction channel being formed below the buried region, and further wherein the buried region is spaced-apart from the drain diffusion region. Rather, in Eklund's device structure a separate n-top layer 28 is formed over an p-type JFET gate control layer 27 that contacts drain diffusion region 24 within a diffused n+ well 21.

As to the statement in the Office Action that column 3, lines 1-62 of Eklund evidences that "impurity concentration is an art-recognized parameter of importance subject to routine experimentation and optimization, and that an impurity concentration of approximately 1 X $10^{12}/cm^2$ is well within the art-recognized range for a doping concentration of a JFET channel", Applicant respectfully submits that no statements regarding impurity concentration are found in the cited passage of the Eklund reference.

Furthermore, an ordinary practitioner would have been discouraged from attempting to incorporate Eklund's JFET gate control layer 27 into Williams' drift layer 521because Williams' teaches forming an extended drift region with a depth less than one micron, which is too shallow to permit formation of a buried region such as Eklund's layer 27 connected to drain diffusion region 24. The same is true with respect to Yamanishi; that is, an ordinary practitioner attempting to combine Williams with Yamanishi would have understood that a one micron deep N-type drift region is too shallow to permit formation of a buried region therein using Yamanishi's method of segregation of dopants by heat treatment. Thus, a person of ordinary skill in the art would therefore have lacked motivation to combine or modify Williams in view of Yamanishi and/or Eklund to produce a device structure that includes conduction channels above and below the buried region disposed within an

epitaxial layer since there would have been no reasonable expectation that such an approach would work.

Colak teaches a lateral double-diffused MOS transistor fabricated in accordance with basic RESURF principles. However, Colak fails to provide any teaching or disclosure missing from Williams, Yamanishi or Eklund that would have motivated one of ordinary skill in the art to arrive at the claimed invention at the time it was made. For instance, even though Colak shows an upper n-type layer 24a separated from an n-type lower layer 14 by a p+ layer 16, Colak specifically teaches that lower layer 14 is isolated from the current-carrying path due to the intervening second semiconductor layer 16 (column 5, lines 52-62).

In this case, there is no logical reason apparent from the cited prior art references for a person of ordinary skill in the art to achieve a high-voltage transistor having a buried layer disposed in an epitaxial layer that forms upper and lower conduction channels. A reasonable expectation of success simply does not exist in the combination of prior art references suggested by the Examiner. While it may have been obvious *to try*, it would not have been obvious *to do*. Obviousness cannot be predicated upon what a person skilled in the art might find obvious to try, but only on what the prior art would have led a person skilled in the art to do.

Accordingly, Applicant respectfully requests that the rejection of claims 93-111 under 35 U.S.C. § 103(a) be withdrawn.

It is respectfully submitted that claims 93-111 are now in condition for allowance.

Please charge any shortages and credit any overcharges to our Deposit Account No. 50-2060.

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the Un States Postal Service as first class mail with sufficient postage in an en addressed to the Commissioner for Patents, Mail Stop RCE, P.O. Box Alexandria, VA 22313-1450 on November 17, 2003.

Caitlin Burgess — November 17, 2003 Date